IN THE CLAIMS:

Please cancel Claims 3 and 13 in their entirety without prejudice nor to disclaim of the subject matters set forth therein.

Please amend Claim 1 as follows:

1. (Presently Amended) A semiconductor device comprising:

a first MOS transistor group including a first gate electrode and a first impurity diffused layer;

a second MOS transistor group including a second gate electrode, which is arranged in parallel with the first gate electrode, and a second impurity diffused layer;

input signal wiring, to which an input signal is applied, disposed between the first MOS transistor group and the second MOS transistor group; and

a conducting portion extending on the first and the second impurity diffused layers for electrically connecting the first and the second gate electrodes to the input signal wiring;

wherein the conducting portion is formed in the same layer as the first and the second gate electrodes and extends from the first gate electrode to the second gate electrode.

2. (Original) The semiconductor device according to claim 1, wherein a silicide layer is formed in each of the first and the second impurity diffused layers at a position spaced apart by a predetermined distance from the first gate electrode or the second gate electrode.

3. (Cancel)

4. (Original) The semiconductor device according to claim 1, further comprising an interlayer insulating layer disposed between the conducting portion and the input signal wiring, the interlayer insulating layer being provided with a contact for electrically connecting the conducting portion to the input signal wiring.

5. (Original) A semiconductor device including first and second MOS transistor groups, each of the first and second MOS transistor groups including gate electrodes disposed substantially in parallel with each other, first and second impurity diffused layers and a silicide layer formed on the first and second impurity diffused layers other than areas thereof in the vicinity of the gate electrodes, the semiconductor device comprising:

a conducting portion extending from each of the gate electrode at least to the impurity diffused layers;

an interlayer insulating layer covering at least the gate electrodes and the impurity diffused layers;

input signal wiring, to which an input signal is applied, formed on the interlayer insulating layer; and

a contact formed in the interlayer insulating layer for electrically connecting the input signal wiring to the conducting portion directly or indirectly,

wherein the contact is formed outside of an active region including the gate electrodes and the impurity diffused layers.

6. (Original) The semiconductor device according to claim 4, further comprising an element isolation layer disposed between the first and the second MOS transistor groups, wherein the input signal wiring is formed above and along the element isolation layer, the conducting portion comprises a plurality of coupling portions, which extend from the gate electrodes to the impurity diffused layers and to the element isolation layer and are coupled with the gate electrodes at different points in a width direction of the gate electrodes, and the contact comprises a plurality of contacts, which connect the coupling portions to the input signal wiring on the element isolation layer.

7. (Original) The semiconductor device according to claim 5, further comprising an element isolation layer disposed between the first and the second MOS transistor groups, wherein the input signal wiring is formed above and along the element isolation layer, the conducting portion comprises a plurality of coupling portions, which extend from the gate electrodes to the impurity diffused layers and to the element isolation layer and are coupled with the gate electrodes at different points in a width direction of the gate electrodes, and the contact comprises a plurality of contacts, which connect the coupling portions to the input signal wiring on the element isolation layer.

8. (Original) The semiconductor device according to claim 5, wherein the conducting portion comprises a plurality of coupling portions, which extend from the gate electrodes to the impurity diffused layers and are coupled with the gate electrodes at different points in a width direction of the gate electrodes, and a wiring portion, which extends in parallel with the gate electrodes from the active region between the pair of gate electrodes to an area outside of the active region and is coupled with the coupling portions.

9. (Original) The semiconductor device according to claim 1, wherein the gate electrodes and the conducting portion comprise polysilicon.

10. (Original) The semiconductor device according to claim 5, wherein the gate electrodes and the conducting portion comprise polysilicon.

11. (Original) The semiconductor device according to claim 1, wherein a silicide layer is formed on the conducting portion.

12. (Original) The semiconductor device according to claim 5, wherein a silicide layer is formed on the conducting portion.

13. (Cancel)

14. (Original) A semiconductor integrated circuit device including a first transistor used in an output circuit and a second transistor used in an internal circuit, wherein

the first transistor comprises: a semiconductor device including first and second MOS transistor groups, each of the first and second MOS transistor groups including gate electrodes disposed substantially in parallel with each other, first and second impurity diffused layers and a silicide layer formed on the first and second impurity diffused layers other than areas thereof in the vicinity of the gate electrodes, the semiconductor device comprising:

a conducting portion extending from each of the gate electrode at least to the impurity diffused layers;

an interlayer insulating layer covering at least the gate electrodes and the impurity diffused layers;

input signal wiring, to which an input signal is applied, formed on the interlayer insulating layer; and

a contact formed in the interlayer insulating layer for electrically connecting the input signal wiring to the conducting portion directly or indirectly,

wherein the contact is formed outside of an active region including the gate electrodes and the impurity diffused layers; and

the second transistor comprises a salicide MOS transistor.